

**BEST AVAILABLE COPY****AMENDMENTS TO THE CLAIMS**

1. (currently amended) A method for etching a silicon on insulator (SOI) substrate, the method comprising:
  - opening a hardmask layer formed on an SOI layer of the SOI substrate;
  - and
  - etching through said SOI layer, a buried insulator layer underneath said SOI layer, and a bulk silicon layer beneath said buried insulator layer using a single etch step, wherein said single etch step is sufficient to etch through said bulk silicon layer to a depth corresponding to a desired deep trench depth.
2. (original) The method of claim 1, wherein said etching is implemented with an HBR,  $\text{NF}_3$  and  $\text{O}_2$  etch chemistry.
3. (original) The method of claim 2, wherein said etch chemistry is applied at a power of about 500 to about 1000 Watts.
4. (original) The method of claim 1, wherein said etching is implemented at a pressure of about 10 to about 150 mTorr.
5. (original) The method of claim 1, wherein said hardmask layer is formed at a thickness so as to accommodate a 1:1 etch selectivity with respect to said buried insulator layer and about a 5:1 to about a 35:1 etch selectivity with respect to said SOI layer and said bulk silicon layer.
6. (original) The method of claim 5, wherein said hardmask layer further comprises:
  - a pad nitride layer formed on said SOI layer; and
  - a borosilicate glass (BSG) oxide layer formed on said pad nitride layer.

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7. (original) The method of claim 6, wherein said hardmask layer is formed at a thickness of about 6,000 Angstroms to about 20,000 Angstroms.

8. (original) The method of claim 6, wherein said hardmask layer is formed at a thickness of about 10,000 Angstroms to about 18,000 Angstroms.

9. (original) The method of claim 5, wherein said buried insulator layer comprises a buried oxide (BOX) layer formed at a thickness of about 120 to about 140 nanometers.

10. (currently amended) A method for forming a deep trench within a silicon on insulator (SOI) substrate, the method comprising:

forming a hardmask layer on an SOI layer of the SOI substrate;  
patterning a desired deep trench pattern in said hardmask layer; and  
etching through said SOI layer, a buried oxide (BOX) layer underneath said SOI layer, and a bulk silicon layer beneath said BOX layer using a single etch step, wherein said single etch step is sufficient to etch through said bulk silicon layer to a depth corresponding to a desired deep trench depth.

11. (original) The method of claim 10, wherein said etching is implemented with an HBR,  $\text{NF}_3$  and  $\text{O}_2$  etch chemistry.

12. (original) The method of claim 11, wherein said etch chemistry is applied at a power of about 500 to about 1000 Watts.

13. (original) The method of claim 10, wherein said etching is implemented at a pressure of about 10 to about 150 mTorr.

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14. (original) The method of claim 10, wherein said hardmask layer is formed at a thickness so as to accommodate a 1:1 etch selectivity with respect to said BOX layer and about a 5:1 to about a 35:1 etch selectivity with respect to said SOI layer and said bulk silicon layer.

15. (original) The method of claim 14, wherein said hardmask layer further comprises:

a pad nitride layer formed on said SOI layer; and  
a borosilicate glass (BSG) oxide layer formed on said pad nitride layer.

16. (original) The method of claim 15, wherein said hardmask layer is formed at a thickness of about 6,000 Angstroms to about 20,000 Angstroms.

17. (original) The method of claim 15, wherein said hardmask layer is formed at a thickness of about 10,000 Angstroms to about 18,000 Angstroms.

18. (original) The method of claim 13, wherein said buried insulator layer comprises a buried oxide (BOX) layer formed at a thickness of about 120 to about 140 nanometers.